CLAIMS

What is claimed is:

1. A counter comprising:

a nonvolatile storage organized in digits having non-uniform bases; and

circuitry to increment a count value represented by the digits in response to an increment command.

2. The counter of claim 1 wherein the nonvolatile storage includes a plurality of blocks of storage cells, each of the digits being stored in a respective one of the blocks.

3. The counter of claim 2 wherein one of the digits spans two or more of the blocks.

4. The counter of claim 2 wherein the nonvolatile storage is a flash erasable programmable read only memory in which a selected block of the plurality of blocks is erased in response to an erase command that identifies the selected block.

5. The counter of claim 1 wherein each of the digits includes a respective number of bits according to its base.

6. The counter of claim 5 wherein the number of bits is equal to the base minus one.

7. The counter of claim 5 wherein the circuitry to increment the count value comprises circuitry to increment one digit of the digits by programming only one bit of the one digit.

8. The counter of claim 7 wherein the circuitry to increment the one digit of the digits comprises circuitry to evaluate bits of the one digit to identify a least significant bit of the one digit that is in an erased state, the least significant bit being the only one bit programmed to increment the one digit.

9. The counter of claim 1 wherein the circuitry includes circuitry to increment one of the digits and to erase each of the digits less significant than the one of the digits.

10. The counter of claim 9 wherein the circuitry to erase each of the digits less significant than the one of the digits comprises circuitry to concurrently erase each of the digits less significant than the one of the digits.

11. The counter of claim 1 wherein the counter is a down counter and wherein the circuitry to increment the count value causes the count value to be reduced by one in response to the increment command.

12. The counter of claim 1 wherein the counter is monotonic, the counter further comprising circuitry to prevent erasure of the digits in response to detecting that a maximum count of the counter has been reached.

13. The counter of claim 1 further comprising configuration circuitry to receive a counter setup command and to allocate regions of the nonvolatile storage to the digits according to the counter setup command.

14. The counter of claim 13 wherein the configuration circuitry is configured to store setup information specified in the setup command in a region of the nonvolatile storage.

15. The counter of claim 14 wherein the region of the nonvolatile storage where the setup information is stored is a one-time programmable region that cannot be erased.

16. The counter of claim 14 further comprising initialization circuitry to read the setup information in the region of the nonvolatile storage to identify the digits of the counter.

17. The counter of claim 1 further comprising:

program circuitry to write data to the nonvolatile storage in response to program commands received from an external source; and

circuitry to detect whether an address specified by one of the program commands falls within a range of the nonvolatile storage allocated to the digits and, if so, to disallow the program circuitry from writing data at the address.

18. The counter of claim 1 further comprising circuitry to output the count value represented by the digits in response to the increment command.

19. The counter of claim 1 further comprising circuitry to output the count value represented by the digits in response to a read counter command.

20. The counter of claim 1 further comprising circuitry to generate a binary representation of the count value for output to a host processor.

21. The counter of claim 20 wherein the circuitry to generate a binary representation of the count value is configured to generate a distinct binary representation of the value of each of the digits.

22. A computer system comprising:
a bus;
a processor coupled to the bus;
a nonvolatile memory device coupled to the bus to receive commands from the processor, the commands including an increment command, the nonvolatile memory device including
a nonvolatile storage array organized in digits having non-uniform bases; and
circuitry to increment a count value represented by the digits in response to the increment command.

23. A computer system comprising:
a bus;
a processor coupled to the bus;
a security co-processor coupled to the bus to receive commands and data from the processor; and

a nonvolatile memory device coupled to receive commands from the security co-processor, the commands including an increment command, the nonvolatile memory device including

a nonvolatile storage array organized in digits having non-uniform bases; and

circuitry to increment a count value represented by the digits in response to the increment command.

24. A method comprising:

receiving a command to increment a counter implemented in a nonvolatile storage device, the nonvolatile storage device including a nonvolatile storage array organized in digits that have non-uniform bases, the digits defining the counter;

searching each of the digits in order of significance until a least significant unprogrammed bit of one of the digits is found; and

programming the unprogrammed bit to carry out the increment command.

25. The method of claim 24 further comprising erasing bits of each of the digits less significant than the one of the digits containing the unprogrammed bit to carry out the increment command.

26. The method of claim 24 further comprising receiving a command specifying a base for each of the digits of the counter.

27. The method of claim 24 further comprising receiving a command specifying a quantity of the digits.